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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,901	11/26/2003	Alain Blanc	FR920020052US1 2914	
25299 IBM CORPOR	7590 11/28/2007 A TION	EXAMINER		
PO BOX 12195	5.	AHMED, SALMAN		
DEPT YXSA, BLDG 002 RESEARCH TRIANGLE PARK, NC 27709			ART UNIT	PAPER NUMBER
			2619	
		,	MAIL DATE	DELIVERY MODE
			11/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
	10/722,901	BLANC ET AL.				
Office Action Summary	Examiner	Art Unit				
	Salman Ahmed	2619				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 26 No.	ovember 2003.					
2a) ☐ This action is FINAL . 2b) ☑ This	action is non-final.					
)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-19</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1,5,6,8 and 15-19</u> is/are rejected.						
7)⊠ Claim(s) <u>2-4,7 and 9-14</u> is/are objected to.						
8) Claim(s) are subject to restriction and/or	r election requirement.					
Application Papers						
9) The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>26 November 2003</u> is/are: a) accepted or b)⊠ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
·						
Attachment(s)						
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date Notice of Informal Patent Application						
Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	6) Other:					

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DETAILED ACTION

Claims 1-19 are pending.

Claims 1, 5, 6, 8 and 15-19 are rejected.

Claims 2-4, 7 and 9-14 are objected to.

Drawings

1. The drawings are objected to because Figure 4 element 401 is corrected/modified to 411. However, it is confusing the way the correction was done, as it is not easily apparent from the drawing that the element number is 411. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

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applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the second paragraph of 35 U.S.C. 112:
 - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claim 6 recites the limitation "the set of wildcard conditions" in line 3. There is insufficient antecedent basis for this limitation in the claim.
- 4. Claim 7 recites the limitation "the corresponding linked list" in line 10. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 5, 6, 8 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wahlman et al. (US PAT 5488453, hereinafter Wahlman) in view of Sharma et al. (US PAT PUB 2002/0064154, hereinafter Sharma).

In regards to claim 1, Wahlman teaches a method for re-sequencing packets comprising: a) in each ingress port-adapter (Figure 4 input unit 3), inserting a packet rank (column 6 lines 50-55 in a field 17 a sequential number, "CSNcell") into each packet to be switched through a parallel packet switch (column 6 lines 50-55, In the unit 7 for the generation of the extra information required for the transfer of a data packet inside the switch 1 a field 17 a sequential number, "CSNcell" is inserted); b) switching the ranked packets through the parallel packet switch; and in each egress port-adapter; c) reading out the switched packets from the parallel packet switch; d) storing the switched packets read out from the parallel packet switch into an egress buffer (column 5 lines 20-30, a data packet which arrives to side A and thus to the input unit 3, generates n identical data packets which are forwarded on the n switching planes, where the communication of these identical data packets are performed totally independently of each other on the different switching planes. These identical data packets then arrive to the output unit 5 (egress port-adapter) and therein correctly transferred data packets are selected and a sequence or stream of output data packets is created having a correct sequential order of the different data packets. Egress buffer

corresponds to unit 23 in conjunction with registers 25); f) selecting the oldest packet of the oldest packets selected and which come from the same ingress port-adapter, according to the value of their packet ranks, for each ingress port-adapter, thereby providing a subset of older packets, each subset corresponding to an ingress port adapter (column 11 lines 5-10, in FIG. 7 a flow diagram is illustrated where the routine starts in a block 501 and thereafter it is asked in a block 503 whether the sequence number "CSNcell" of the considered cell is equal to the expected sequential number "CSNexp" (oldest packet) of the next data packet, which, at the output side of the switch 1, is to be received on this plane for this connection); g) validating the content of each subset; and h) selecting the packet to exit the egress port-adapter among the subsets validated in g) (Figure 6, column 10 lines 25-28 and Figure 12, column 13 lines 48-57, it is considered in a block 413, whether there is any error in the data packet field 11 carrying the proper information "Payload", by checking an indication inside the packet if this check sum "PEC", i.e. the check sum related to the field "Payload", has been corrected. Further, if the check sum (HEC) is determined to be correct, the data packet is allowed to pass to the output buffer 31 in a block 1211).

Wahlman does not explicitly teach e) selecting the oldest packet of each of sets of packets, each set being comprised of packets coming from the same switching plane and the same ingress port-adapter. Wahlman does not explicitly teach multiple packets being utilized as subsets.

Sharma in the same field of endeavor teaches first, data packets of the input flows f.sub.1j-f.sub.nj for j=1-n, are selectively routed to an input data buffer (data

queue) for a switch input port (207, 208, 210, 212) having the shortest data packet pendant time (or smallest amount of stored, pending data i.e. selecting the oldest packet of each of sets of packets) and from which the cross bar switch will route data to an appropriate output port (by provisioning the switch matrices within the cross bar switches) as indicated by the input 308 and output 310 address/port fields of the header 304. Secondly, data is read from the buffer into which the packets were read according to a time stamp 306 in the header such that the "oldest" data cells of a data flow in a buffer are read from that buffer first. By reading the time stamp 306 of a first cell in the FIFOs, the global scheduler 206 reads the oldest cell for each flow first, followed by successively less-old cells, thereby preserving the order in which cells of a data flow are switched, y combining "minimum length demultiplexing" with "k-parallel scheduling," the global scheduler ensures that the k oldest cells of each flow f i,j are always in distinct crossbar switches. This property also ensures that, at the end of each cell slot, for any output i of the super switch, the oldest cell destined for that output is always at the head of one of the output buffers in the k parallel crossbars that hold cells destined for output j. i.e. i.e. selecting the oldest packet of each of sets of packets as subsets (section 0025, 0034 and 0045). Sharma further teaches the output multiplexers 242 and 244 are 2-X-1 multiplexers which also operate under the control of the global scheduler to read data from the output buffers 250, 252, 254, 256 in such fashion that the ordering of data packets of a particular flow that was input to the super switch 200 through either one of the inputs 246 and 248 is preserved when the data is read out of the switch from either one of or both of the output multiplexers 242 and 244 (section 0052).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Wahlman's packet sequencing method using sequence field by incorporating timestamp sequencing method for packet re-sequencing as suggested by Sharma. The motivation is that, such method of dual re-sequencing method would ensure reliable and efficient packet ordering through high-speed switches, i.e. as suggested by Sharma, (section 0014) by appropriately configuring circuitry to direct high-speed data into multiple cross bar switches, it is possible to perform the operation of a single, very high speed cross bar switch albeit using several lower speed, lower cost switches, without mis-ordering data packets that are routed through the separate switch matrices.

In regards to claim 5, Wahlman teaches validating a subset of older packets originated from a same ingress port-adapter (Figure 6, column 10 lines 25-28 and Figure 12, column 13 lines 48-57, it is considered (validating) in a block 413, whether there is any error in the data packet field 11 carrying the proper information "Payload", by checking an indication inside the packet if this check sum "PEC", i.e. the check sum related to the field "Payload", has been corrected) when either one of the valid condition (Figure 6 block 409, measure and evaluate quality in regard of sequential correctness for data packets) or corresponding wildcard condition is valid for all switching planes.

In regards to claim 6, Wahlman teaches i) forwarding the packet selected in h) (Figure 6, column 10 lines 25-28 and Figure 12, column 13 lines 48-57, it is considered in a block 413, whether there is any error in the data packet field 11 carrying the proper information "Payload", by checking an indication inside the packet if this check sum

"PEC", i.e. the check sum related to the field "Payload", has been corrected. Further, if the check sum (HEC) is determined to be correct, the data packet is allowed to pass to the output buffer 31 in a block 1211); and j) resetting the set of wildcard conditions associated to the same ingress adapter as the forwarded packet (column 7 lines 14-17, then the sequential numbers are restarted from the beginning. The sequential numbers will thus return cyclically).

In regards to claim 8, Wahlman teaches a method for re-sequencing packets carrying a priority which have been switched through the parallel packet switch comprising: a) in each ingress port-adapter (Figure 4 input unit 3), inserting a packet rank (column 6 lines 50-55 in a field 17 a sequential number, "CSNcell") into each packet to be switched through the parallel packet switch (column 6 lines 50-55, In the unit 7 for the generation of the extra information required for the transfer of a data packet inside the switch 1 a field 17 a sequential number, "CSNcell" is inserted); b) switching the ranked packets through the parallel packet switch; and in each egress port-adapter: c) reading out the switched packets from the parallel packet switch; d) storing the switched packets read out from the parallel packet switch into an egress buffer (column 5 lines 20-30, a data packet which arrives to side A and thus to the input unit 3, generates n identical data packets which are forwarded on the n switching planes, where the communication of these identical data packets are performed totally independently of each other on the different switching planes. These identical data packets then arrive to the output unit 5 (egress port-adapter) and therein correctly transferred data packets are selected and a sequence or stream of output data packets

is created having a correct sequential order of the different data packets. Egress buffer corresponds to unit 23 in conjunction with registers 25); f) selecting the oldest packet of the oldest packets selected in e) and which come from the same ingress port-adapter with the same priority, according to the value of their packet ranks, for each ingress port-adapter and each priority, thereby providing a subset of older packets, each subset corresponding to an ingress port-adapter and a priority (column 11 lines 5-10, in FIG. 7 a flow diagram is illustrated where the routine starts in a block 501 and thereafter it is asked in a block 503 whether the sequence number "CSNcell" of the considered cell is equal to the expected sequential number "CSNexp" (oldest packet) of the next data packet, which, at the output side of the switch 1, is to be received on this plane for this connection); g) validating the content of each subset; and h) selecting the packet to exit the egress port-adapter among the subsets validated in g) (Figure 6, column 10 lines 25-28 and Figure 12, column 13 lines 48-57, it is considered in a block 413, whether there is any error in the data packet field 11 carrying the proper information "Payload", by checking an indication inside the packet if this check sum "PEC", i.e. the check sum related to the field "Payload", has been corrected. Further, if the check sum (HEC) is determined to be correct, the data packet is allowed to pass to the output buffer 31 in a block 1211).

Wahlman does not explicitly teach selecting the oldest packet of each sets of packets stored each set being comprised of packets coming from the same switching plane, the same ingress port-adapter with the same priority. Wahlman does not explicitly teach multiple packets being utilized as subsets.

Sharma in the same field of endeavor teaches first, data packets of the input flows f.sub.1j-f.sub.nj for j=1-n, are selectively routed to an input data buffer (data queue) for a switch input port (207, 208, 210, 212) having the shortest data packet pendant time (or smallest amount of stored, pending data i.e. selecting the oldest packet of each of sets of packets) and from which the cross bar switch will route data to an appropriate output port (by provisioning the switch matrices within the cross bar switches) as indicated by the input 308 and output 310 address/port fields of the header 304. Secondly, data is read from the buffer into which the packets were read according to a time stamp 306 in the header such that the "oldest" data cells of a data flow in a buffer are read from that buffer first (same priority). By reading the time stamp 306 of a first cell in the FIFOs, the global scheduler 206 reads the oldest cell for each flow first, followed by successively less-old cells, thereby preserving the order in which cells of a data flow are switched. y combining "minimum length demultiplexing" with "k-parallel scheduling," the global scheduler ensures that the k oldest cells of each flow f i,j are always in distinct crossbar switches. This property also ensures that, at the end of each cell slot, for any output j of the super switch, the oldest cell destined for that output is always at the head of one of the output buffers in the k parallel crossbars that hold cells destined for output j. i.e. i.e. selecting the oldest packet of each of sets of packets as subsets (section 0025, 0034 and 0045). Sharma further teaches the output multiplexers 242 and 244 are 2-X-1 multiplexers which also operate under the control of the global scheduler to read data from the output buffers 250, 252, 254, 256 in such fashion that the ordering of data packets of a particular flow that was input to the super switch 200

through either one of the inputs 246 and 248 is preserved when the data is read out of the switch from either one of or both of the output multiplexers 242 and 244 (section 0052).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Wahlman's packet sequencing method using sequence field by incorporating timestamp sequencing method for packet re-sequencing as suggested by Sharma. The motivation is that, such method of dual re-sequencing method would ensure reliable and efficient packet ordering through high-speed switches, i.e. as suggested by Sharma, (section 0014) by appropriately configuring circuitry to direct high-speed data into multiple cross bar switches, it is possible to perform the operation of a single, very high speed cross bar switch albeit using several lower speed, lower cost switches, without mis-ordering data packets that are routed through the separate switch matrices.

In regards to claim 15, Wahlman teaches a system comprising: a parallel packet switch (Figure 3, Switching Planes 1 and 2); at least one ingress adapter (Figure 3, Input Unit 3n) operably coupled to the parallel packet switch; at least one egress adapter (Figure 3, Output Unit 5n) operably coupled to the parallel packet switch wherein at least one ingress adapter inserts a packet rank (column 6 lines 50-55, In the unit 7 for the generation of the extra information required for the transfer of a data packet inside the switch 1 a field 17 a sequential number, "CSNcell" is inserted) into each packet to be switched through packet switch and at least one egress adapter receiving switched packets (column 5 lines 20-30, a data packet which arrives to side A

and thus to the input unit 3, generates n identical data packets which are forwarded on the n switching planes, where the communication of these identical data packets are performed totally independently of each other on the different switching planes. These identical data packets then arrive to the output unit 5 (egress port-adapter) and therein correctly transferred data packets are selected and a sequence or stream of output data packets is created having a correct sequential order of the different data packets. Egress buffer corresponds to unit 23 in conjunction with registers 25), forming subset of packets based upon predefined characteristics from set of packets (column 11 lines 5-10, in FIG. 7 a flow diagram is illustrated where the routine starts in a block 501 and thereafter it is asked in a block 503 whether the sequence number "CSNcell" of the considered cell is equal to the expected sequential number "CSNexp" (predefined characteristics) of the next data packet, which, at the output side of the switch 1, is to be received on this plane for this connection), validating contents of each subset and selecting a packet to exit at least one egress adapter from the subset so validated (Figure 6, column 10 lines 25-28 and Figure 12, column 13 lines 48-57, it is considered in a block 413, whether there is any error in the data packet field 11 carrying the proper information "Payload", by checking an indication inside the packet if this check sum "PEC", i.e. the check sum related to the field "Payload", has been corrected. Further, if the check sum (HEC) is determined to be correct, the data packet is allowed to pass to the output buffer 31 in a block 1211).

Wahlman does not explicitly teach forming first set of packets from received switched packets. Wahlman does not explicitly teach multiple packets being utilized as subsets.

Sharma in the same field of endeavor teaches first, data packets of the input flows f.sub.1j-f.sub.nj for j=1-n, are selectively routed to an input data buffer (data queue) for a switch input port (207, 208, 210, 212) having the shortest data packet pendant time (or smallest amount of stored, pending data i.e. selecting the oldest packet of each of sets of packets) and from which the cross bar switch will route data to an appropriate output port (by provisioning the switch matrices within the cross bar switches) as indicated by the input 308 and output 310 address/port fields of the header 304. Secondly, data is read from the buffer into which the packets were read according to a time stamp 306 in the header such that the "oldest" data cells of a data flow in a buffer are read from that buffer first. By reading the time stamp 306 of a first cell in the FIFOs, the global scheduler 206 reads the oldest cell for each flow first, followed by successively less-old cells, thereby preserving the order in which cells of a data flow are switched. y combining "minimum length demultiplexing" with "k-parallel scheduling," the global scheduler ensures that the k oldest cells of each flow f_i,j are always in distinct crossbar switches. This property also ensures that, at the end of each cell slot, for any output j of the super switch, the oldest cell destined for that output is always at the head of one of the output buffers in the k parallel crossbars that hold cells destined for output j. i.e. i.e. selecting the oldest packet of each of sets of packets as subsets (section 0025, 0034 and 0045). Sharma further teaches the output multiplexers 242 and 244 are Application/Control Number: 10/722,901

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2-X-1 multiplexers which also operate under the control of the global scheduler to read data from the output buffers 250, 252, 254, 256 in such fashion that the ordering of data packets of a particular flow that was input to the super switch 200 through either one of the inputs 246 and 248 is preserved when the data is read out of the switch from either one of or both of the output multiplexers 242 and 244 (section 0052).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Wahlman's packet sequencing method using sequence field by incorporating timestamp sequencing method for packet re-sequencing as suggested by Sharma. The motivation is that, such method of dual re-sequencing method would ensure reliable and efficient packet ordering through high-speed switches, i.e. as suggested by Sharma, (section 0014) by appropriately configuring circuitry to direct high-speed data into multiple cross bar switches, it is possible to perform the operation of a single, very high speed cross bar switch albeit using several lower speed, lower cost switches, without mis-ordering data packets that are routed through the separate switch matrices.

In regards to claims 16 and 17, Wahlman teaches the first set of packets includes oldest packet from sets of packets received in at least egress adapter wherein each set being comprised of packets coming from same switching plane within parallel switch and same at least one ingress adapter and the predefined characteristics include the oldest of packets in the first set (column 5 lines 20-30 and column 11 lines 5-10, a data packet which arrives to side A and thus to the input unit 3, generates n identical data packets which are forwarded on the n switching planes, where the communication

of these identical data packets are performed totally independently of each other on the different switching planes. These identical data packets then arrive to the output unit 5 (egress port-adapter) and therein correctly transferred data packets are selected and a sequence or stream of output data packets is created having a correct sequential order of the different data packets. Egress buffer corresponds to unit 23 in conjunction with registers 25. In FIG. 7 a flow diagram is illustrated where the routine starts in a block 501 and thereafter it is asked in a block 503 whether the sequence number "CSNcell" of the considered cell is equal to the expected sequential number "CSNexp" (oldest packet) of the next data packet, which, at the output side of the switch 1, is to be received on this plane for this connection).

In regards to claim 18, Wahlman teaches a method for resequencing packets comprising: a) receiving in at least one egress adapter switched packets (column 5 lines 20-30, a data packet which arrives to side A and thus to the input unit 3, generates n identical data packets which are forwarded on the n switching planes, where the communication of these identical data packets are performed totally independently of each other on the different switching planes. These identical data packets then arrive to the output unit 5 (egress port-adapter) and therein correctly transferred data packets are selected and a sequence or stream of output data packets is created having a correct sequential order of the different data packets. Egress buffer corresponds to unit 23 in conjunction with registers 25); b) selecting oldest packet from packets, each set being comprised of packets coming from a common switching plane and a common ingress adapter (column 11 lines 5-10, in FIG. 7 a flow diagram is illustrated where the routine

starts in a block 501 and thereafter it is asked in a block 503 whether the sequence number "CSNcell" of the considered cell is equal to the expected sequential number "CSNexp" (oldest packet) of the next data packet, which, at the output side of the switch 1, is to be received on this plane for this connection).

Wahlman does not explicitly teach and c) selecting oldest packet of the oldest packets selected in b) to provide a subset of oldest packets. Wahlman does not explicitly teach multiple packets being utilized as subsets.

Sharma in the same field of endeavor teaches first, data packets of the input flows f.sub.1j-f.sub.nj for j=1-n, are selectively routed to an input data buffer (data queue) for a switch input port (207, 208, 210, 212) having the shortest data packet pendant time (or smallest amount of stored, pending data i.e. selecting the oldest packet of each of sets of packets) and from which the cross bar switch will route data to an appropriate output port (by provisioning the switch matrices within the cross bar switches) as indicated by the input 308 and output 310 address/port fields of the header 304. Secondly, data is read from the buffer into which the packets were read according to a time stamp 306 in the header such that the "oldest" data cells of a data flow in a buffer are read from that buffer first (i.e. oldest packet of the oldest packets among different buffers are selected). By reading the time stamp 306 of a first cell in the FIFOs, the global scheduler 206 reads the oldest cell for each flow first, followed by successively less-old cells, thereby preserving the order in which cells of a data flow are switched, y combining "minimum length demultiplexing" with "k-parallel scheduling," the global scheduler ensures that the k oldest cells of each flow f_i,j are always in distinct

crossbar switches. This property also ensures that, at the end of each cell slot, for any output j of the super switch, the oldest cell destined for that output is always at the head of one of the output buffers in the k parallel crossbars that hold cells destined for output j. i.e. i.e. selecting the oldest packet of each of sets of packets as subsets (section 0025, 0034 and 0045). Sharma further teaches the output multiplexers 242 and 244 are 2-X-1 multiplexers which also operate under the control of the global scheduler to read data from the output buffers 250, 252, 254, 256 in such fashion that the ordering of data packets of a particular flow that was input to the super switch 200 through either one of the inputs 246 and 248 is preserved when the data is read out of the switch from either one of or both of the output multiplexers 242 and 244 (section 0052).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Wahlman's packet sequencing method using sequence field by incorporating timestamp sequencing method for packet re-sequencing as suggested by Sharma. The motivation is that, such method of dual re-sequencing method would ensure reliable and efficient packet ordering through high-speed switches, i.e. as suggested by Sharma, (section 0014) by appropriately configuring circuitry to direct high-speed data into multiple cross bar switches, it is possible to perform the operation of a single, very high speed cross bar switch albeit using several lower speed, lower cost switches, without mis-ordering data packets that are routed through the separate switch matrices.

In regards to claim 19, Wahlman teaches validating contents of each subset; and selecting a packet to exit among the subsets so validated (Figure 6, column 10 lines 25-

28 and Figure 12, column 13 lines 48-57, it is considered in a block 413, whether there is any error in the data packet field 11 carrying the proper information "Payload", by checking an indication inside the packet if this check sum "PEC", i.e. the check sum related to the field "Payload", has been corrected. Further, if the check sum (HEC) is determined to be correct, the data packet is allowed to pass to the output buffer 31 in a block 1211).

Allowable Subject Matter

- 8. Claims 2, 3, 4, 9-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 9. Claim 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571) 272-8307. The examiner can normally be reached on 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.' Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SA Salman Ahmed Patent Examiner 11/16/2007

> EDAN . ORGAD SUPERVISORY PATENT EXAMINER